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| 09/579,646 | 05/26/2000 | Katsufumi Nakamura | A0312/7363/RJP | 8011 |

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| EXAMINER | |
|---|---|
| AGGARWAL, YOGESH K | |
| **ART UNIT** | **PAPER NUMBER** |
| 2615 | |

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/579,646 | NAKAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Yogesh K. Aggarwal | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2 and 4-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/22/2005 has been entered.

***Response to Arguments***

2. Applicant's arguments with respect to claims 1, 9 and 10 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US Patent # 5,703,524).

[Claim 1]

Chen discloses a programmable gain amplifier (figure 11) having an amplifier that has an input and output that has two phases control signals $\phi_1$ and $\phi_2$ used to control the gain. When $\phi_1$ is high (read as first time phase) an input voltage is sampled on to a sampling capacitor $C_S$ (input capacitor) and a reference voltage (in this case ground) is sampled onto a feedback capacitor $C_F$

i.e. coupled between the input and output of the amplifier. When $\phi_2$ is high (read as a second time phase or amplifying time phase) an output voltage is sampled onto the feedback capacitor $C_F$. Examiner notes that Sampling capacitor $C_S$ (input capacitor) is functionally coupled to the input of the amplifier during the first and second time phases.

[Claim 2]

The symbol denoted for $C_S$ (input capacitor) denotes a variable capacitor.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 9-12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Domer et al. (US Patent # 6,346,968).

[Claim 9]

Domer et al. teaches a method of amplifying input pixels comprising the steps of sampling an input pixel during a first time phase (e.g. during T1, the switches of programmable capacitors 320 and 330 are enabled by first CONTROL data from the lookup table in memory 212 to set the values of programmable capacitors 320 and 330 i.e. input pixel signals are sampled, col. 5 lines 35-46, figures 3 and 4) and amplifying the sampled input pixel during the second time phase (e.g. during T2, switches 314-315 are closed to operate PGA 204 in a gain mode during which

VOUT is valid i.e. sets the gain for the first pixel, col. 5 lines 46-51). Domer further teaches that color balancing is achieved by adjusting the gain of the PGA 204 with CONTROL data mapped to each pixel and stored in the lookup table of memory 212 (col. 3 lines 40-48). Domer also teaches that CONTROL data is provided at the pixel rate and therefore calculations that are too complex to be performed on each cycle of Vpixel are updated in buffer memory 212 (col. 3 line 66-col. 4 line 21) and therefore reads on controlling a gain of the amplification of the input pixel at the pixel rate in response to a gain control signal comprising information related to a desired gain.

[Claim 10]

Domer et al. teaches a PGA (figures 2 and 3, PGA 204) to color balancing the pixels in an image capturing system. Domer futher teaches that during T1, the switches of programmable capacitors 320 and 330 are enabled by first CONTROL data from the lookup table in memory 212 to set the values of programmable capacitors 320 and 330 and during T2, switches 314-315 are closed to operate PGA 204 in a gain mode during which VOUT is valid (sets the gain for the first pixel, col. 5 lines 35-51). Similarly during T3 and T4, the switches of programmable capacitors 320 and 330 are enabled by SECOND CONTROL data from the lookup table in memory 212 to set the values of programmable capacitors 320 and 330 and a gain mode in which Vout signal is valid (sets the gain for the second pixel, col. 5 lines 52-67).

[Claims 11 and 14]

Domer teaches programmable capacitors 320 and 330 used to vary the gain (col. 5 lines 35-67).

[Claim 12]

Domer et al. changes the gain for a first and second pixel, which are successive pixels (col. 5 lines 20-34). Therefore the rate is changed at the input pixel rate.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent # 5,703,524).

[Claim 17]

Chen discloses a variable input capacitor and a feedback capacitor to be used in a programmable gain amplifier. Official Notice is taken of the fact that an input capacitor and a feedback capacitor is very well known in the art to be used to determine the variable gain of a PGA in order to control the gain of the PGA easily. Therefore taking the combined teachings of Chen and Official Notice, it would be obvious to one skilled in the art to have been motivated to have used an input capacitor and a feedback capacitor to determine the variable gain of a PGA in order to control the gain of the PGA easily for each pixel.

[Claim 19]

Chen discloses a PGA but fails to disclose wherein the charge sampled onto the input capacitor comprises charge corresponding to pixel data and charge corresponding to reset noise. Official Notice is taken of the fact that PGAs as described in Chen are notoriously used to amplify the analog pixels generated by a CCD (or MOS pixel) devices and a CDS circuit that introduces

some reset noise and therefore the input capacitor comprises charge corresponding to pixel data and reset noise. Therefore taking the combined teachings of Chen and Official Notice, it would be obvious to one skilled in the art to have been motivated to have the charge sampled onto the input capacitor being comprised of charges corresponding to pixel data and charge corresponding to reset noise in order to amplify the different pixels by a variable gain.

9. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent # 5,703,524) in view of (USPN 6,529,237 to Tsay et al.).

[Claim 4]

Chen teaches the limitations of claim 1 including a variable input capacitor but fails to disclose wherein a capacitance of the input capacitor changes at a rate corresponding to a rate at which pixels are input into the circuit.

However Tsay discloses the pixel gain amplifier circuit of claim 2 wherein a capacitance of the input capacitor changes at a rate corresponding to a rate at which pixels are input into the circuit (e.g., Tsay discloses to provide a variable capacitance input capacitor so as to enable a programmable gain function wherein implicit to the device, the gain can be changed for each pixel, i.e., at a rate corresponding to a rate at which pixels are input into the circuit; column 6, lines 4-9).

Therefore taking the combined teachings of Chen and Tsay, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a capacitance of the input capacitor changes at a rate corresponding to a rate at which pixels are input into the circuit in order to have synchronization between the input pixel rate and the input capacitor rate.

[Claim 5]

Chen discloses the limitation of claim 1 but fails to disclose that the feedback capacitor includes a variable capacitor.

However Examiner notes that in Tsay, according to equation 3 disclosed in column 6 it is functionally equivalent to vary the capacitance of the feedback capacitors Cf in order to effect an adjustment to the gain of the amplifier. As such, it would have been well within the level of one skilled in the art to select to make either the Csm and Csp capacitors or the Cf capacitor variable in order to adjust the gain of the amplifier.

Therefore taking the combined teachings of Chen and Tsay, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a PGA having a variable feedback capacitor in order to adjust the gain of the amplifier.

[Claim 6]

Examiner notes that Tsay disclosed to make capacitors variable through the use of a capacitor array as shown in Fig. 5.

[Claim 7]

In regards to claim 7 note that Tsay discloses to provide a variable capacitance input capacitor so as to enable a programmable gain function wherein inherent to the device, the gain can be changed for each pixel, i.e., at a rate corresponding to a rate at which pixels are input into the circuit (e.g., column 6, lines 4-9).

10. Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent # 5,703,524) in view of Panicacci et al. (US PG-PUB # 2005/0195645).

[Claims 8 and 13]

Chen fails to disclose an offset correction circuitry wherein an input of the offset correction circuit is coupled to the output of the amplifier and an output of the offset correction circuit is coupled to the input of the amplifier. However Panicacci et al. teaches that an amplifier circuit 66 (figure 4a) that includes additional circuitry for reducing or eliminating an offset of the operational amplifier 90. The additional circuitry includes the capacitor C7 and switches S11, S12, S13, with common poles of the switches S11 and S13 held at the reference voltage Vcl (Paragraph 50).

Therefore taking the combined teachings of Chen and Panicacci, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an offset correction circuitry wherein an input of the offset correction circuit is coupled to the output of the amplifier and an output of the offset correction circuit is coupled to the input of the amplifier as taught in Panicacci to be used in the PGA of Chen in order to reduce the offset voltages that is generated by quiescent carrier generation in the photoactive devices as well as offsets from imperfect component matching in CDS and PGA.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent # 5,703,524) in view of Domer et al. (US Patent # 6,346,968).

[Claim 18]

Chen fails to teach changing said gain at the pixel rate. However Domer teaches that CONTROL data is provided at the pixel rate (col. 3 line 66-col. 4 line 21) so that the gain changes at the pixel rate. Therefore taking the combined teachings of Chen and Domer, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a gain that

changes at the input pixel rate in order to have synchronization between the input pixel rate and the gain.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Domer et al. (US Patent # 6,346,968) in view of (USPN 6,529,237 to Tsay et al.).

[Claim 15]

See Examiner notes regarding rejection of claim 5.

13. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Domer et al. (US Patent # 6,346,968) in view of Panicacci et al. (US PG-PUB # 2005/0195645).

[Claim 16]

See Examiner notes regarding rejection of claims 8 and 13.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
November 11, 2005

DAVID L. OMETZ
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EXAMINER